ABSTRACT

A transparent port which maps continuous format signals of an arbitrary rate into frames of a pre-selected single common rate, is provided with a programmable link termination/instigation, for example a FPGA. The port identifies the rate of the continuous signal, recognizes its protocol and the FPGA is configured accordingly. FPGA performs framing, counts errors, does code conversion, corrects parity and performs any other performance monitoring specific to the protocol. In this way, the continuous format signal may be carried transparently as a tributary of e.g. a SONET network, and the performance parameters for the previous section, such as the previous section fail, may be reported to the far end.